# **WEST Search History**

Hide Items Restore Clear Cancel

DATE: Monday, September 13, 2004

Hide?	Set Name	Query	<b>Hit Count</b>
	DB=PGPI	B, USPT, USOC, EPAB, JPAB, DWPI, TDBD; PLUR=YES	; OP=ADJ
	L12	110 and (134/183 or 134/182 or 134/99.1).ccls.	16
	L11	L9 and (single type)	13
	L10	L9 and single\$	1227
	L9	L8 and semiconductor	3202
	L8	cleaning apparatus	29396

**END OF SEARCH HISTORY** 

# **WEST Search History**

Hide Items Restore Clear Cancel

DATE: Monday, September 13, 2004

Hide?	Set Name	Query	Hit Count
	DB=PGPB,U	${\it JSPT, USOC, EPAB, JPAB, DWPI, TDBD; PLUR} =$	YES; OP=ADJ
	L7	L5 and concrete	18
	L6	L5 and (concrete waste)	0
	L5	L4 and (not adher\$)	312
	L4	L3 and polymer\$	502
	L3	L2 and liner	3003
	L2	220/\$.ccls. and container	40904
	L1	220/\$.ccls. and (washout container)	0

END OF SEARCH HISTORY

e

## **Hit List**

Clear Generate Collection Print Fwd Refs Bkwd Refs
Generate OACS

Search Results - Record(s) 11 through 13 of 13 returned.

11. Document ID: US 5608136 A

Using default format because multiple data bases are involved.

L11: Entry 11 of 13

File: USPT

Mar 4, 1997

US-PAT-NO: 5608136

DOCUMENT-IDENTIFIER: US 5608136 A

TITLE: Method and apparatus for pyrolytically decomposing waste plastic

DATE-ISSUED: March 4, 1997

INVENTOR-INFORMATION:

NAME CITY ZIP CODE STATE COUNTRY Maezawa; Yukishige Tokyo J₽ Hayata; Terunobu Kanagawa-ken JΡ Shimada; Hideki Kanagawa-ken JP Ito; Isao Chiba-ken JΡ Suzuki; Kazuo Tokyo JP Tadauchi; Masahiro Tokyo JΡ Tezuka; Fuminobu Tokyo JP Kano; Jiro Tokyo JΡ

US-CL-CURRENT: <u>588/228</u>; <u>201/2.5</u>, <u>585/241</u>, <u>588/213</u>, <u>588/216</u>

Full Title Citation	Front Review Classif	ication Date Referen	68	Claims KWC Draw De

12. Document ID: KR 2004015440 A

L11: Entry 12 of 13

File: DWPI

Feb 19, 2004

DERWENT-ACC-NO: 2004-458969

DERWENT-WEEK: 200443

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TITLE: Forming wiring in semiconductor manufacture

INVENTOR: HONG, U S; PARK, B R

PRIORITY-DATA: 2002KR-0047690 (August 13, 2002)

PATENT-FAMILY:

PUB-NO PUB-DATE

LANGUAGE

PAGES MAIN-IPC

 $h \qquad \quad e \ b \qquad \quad b \ cg \ b \quad cc \qquad \quad e$ 

KR 2004015440 A February 19, 2004

001

H01L021/28

INT-CL (IPC):  $\underline{\text{H01}}$   $\underline{\text{L}}$   $\underline{21/28}$ 

Full Title Citation Front Review Classification Date Reference

### 13. Document ID: KR 416592 B, US 20020108641 A1, JP 2002305175 A, KR 2002066448 A, TW 529069 A

L11: Entry 13 of 13

File: DWPI

Feb 5, 2004

DERWENT-ACC-NO: 2003-016043

DERWENT-WEEK: 200437

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TITLE: Semiconductor wafer cleaning apparatus includes gas spraying unit with

injection tube oriented to inject gas towards wafer

INVENTOR: HA, S R; HAN, Y P; LEE, G T; HAH, S R; HAH, S; HAN, Y; LEE, K

PRIORITY-DATA: 2001KR-0006623 (February 10, 2001)

### PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 416592 B	February 5, 2004		000	H01L021/304
US 20020108641 A1	August 15, 2002		009	B08B003/02
JP 2002305175 A	October 18, 2002		007	H01L021/304
KR 2002066448 A	August 17, 2002		000	H01L021/304
TW 529069 A	April 21, 2003		000	H01L021/00

INT-CL (IPC):  $\underline{B08} \ \underline{B} \ \underline{3/02}; \ \underline{B08} \ \underline{B} \ \underline{5/00}; \ \underline{H01} \ \underline{L} \ \underline{21/00}; \ \underline{H01} \ \underline{L} \ \underline{21/304}$ 

Generate Collection   Print   Fwd Refs   Bkv	wd Refs   Generate
Term	Documents
SINGLE	3297841
SINGLES	3115
ТҮРЕ	5635300
TYPES	1743634
(9 AND (SINGLE ADJ TYPE)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	13

## **Hit List**

Clear Generate Collection Print Fwd Refs Bkwd Refs
Generate OACS

Search Results - Record(s) 11 through 16 of 16 returned.

11. Document ID: US 6668844 B2

Using default format because multiple data bases are involved.

L12: Entry 11 of 16

File: USPT

Dec 30, 2003

US-PAT-NO: 6668844

DOCUMENT-IDENTIFIER: US 6668844 B2

TITLE: Systems and methods for processing workpieces

DATE-ISSUED: December 30, 2003

INVENTOR-INFORMATION:

NAME CITY STATE ZIP CODE COUNTRY Lund; Eric WA Kent Lanfrankie; Joe Kent WA Lund; Gil Kent WA Scranton; Dana Kalispell MT Bergman; Eric Kalispell MT

US-CL-CURRENT: <u>134/155</u>; <u>134/137</u>, <u>134/186</u>, <u>134/30</u>, <u>134/33</u>, <u>134/902</u>, <u>134/99.1</u>, <u>34/165</u>, <u>34/279</u>, <u>34/288</u>, <u>34/397</u>, <u>34/444</u>

Full Title Citation Front Review Classification Date Reference Claims MMC Graw De

12. Document ID: US 6536452 B1

L12: Entry 12 of 16

File: USPT

Mar 25, 2003

US-PAT-NO: 6536452

DOCUMENT-IDENTIFIER: US 6536452 B1

TITLE: Processing apparatus and processing method

DATE-ISSUED: March 25, 2003

INVENTOR-INFORMATION:

NAME CITY STATE ZIP CODE COUNTRY Kohama; Kyouji Hachioji JΡ Shimbo; Eiji Tokyo-To JΡ Kamikawa; Yuji Koshi-Machi JΡ Toshima; Takayuki Yamanashi-Ken JP

h e b b cg b cc e

Ohno; Hiroki

Machida

J₽

US-CL-CURRENT:  $\underline{134}/\underline{117}$ ;  $\underline{134}/\underline{148}$ ,  $\underline{134}/\underline{157}$ ,  $\underline{134}/\underline{183}$ ,  $\underline{134}/\underline{200}$ ,  $\underline{134}/\underline{902}$ 

#### ABSTRACT:

A processing apparatus essentially includes a rotatable rotor 21 for carrying semiconductor wafers W, a motor 22 for driving to rotate the rotor 21, a plurality of processing chambers for surrounding the wafers W carried by the rotor 21, for example, an inner chamber 23 and an outer chamber 24, a chemical supplying unit 50, an IPA supplying unit 60, a rinse supplying unit 70 and a drying fluid supplying unit 80. With this constitution of the apparatus, it is possible to prevent the wafers from being contaminated due to the reaction of treatment liquids of different kinds, with the improvement of processing efficiency and miniaturization of the apparatus.

30 Claims, 24 Drawing figures Exemplary Claim Number: 14 Number of Drawing Sheets: 21

Full Title Citation Front Review Cla	assification   Date   Reference	Claims KWC Draw De
***************************************		

13. Document ID: US 6261427 B1

L12: Entry 13 of 16

File: USPT

Jul 17, 2001

US-PAT-NO: 6261427

DOCUMENT-IDENTIFIER: US 6261427 B1

TITLE: System for fabricating lithographic stencil masks

DATE-ISSUED: July 17, 2001

INVENTOR-INFORMATION:

NAME

CITY

STATE

ZIP CODE

COUNTRY

Rolfson; J. Brett

Boise ID

US-CL-CURRENT: 204/224M; 134/182, 134/94.1, 134/99.1

### ABSTRACT:

A method, apparatus and system for fabricating a stencil mask for ion beam and electron beam lithography are provided. The stencil mask includes a silicon substrate, a membrane formed from the substrate, and a mask pattern formed by through openings in the membrane. The method includes defining the mask pattern and membrane area using <u>semiconductor</u> fabrication processes, and then forming the membrane by back side etching the substrate. The apparatus is configured to electrochemically wet etch the substrate, and to equalize pressure on either side of the substrate during the etch process. The system includes an ion implanter for defining a membrane area on the substrate, optical or e-beam pattern generators for patterning various masks on the substrate, a reactive ion etcher for etching the mask pattern in the substrate, and the apparatus for etching the back side of the substrate.

16 Claims, 17 Drawing figures Exemplary Claim Number: 5 Number of Drawing Sheets: 3

Full: Title: Citation Front Review Classification Date Reference

14. Document ID: US 6110331 A

L12: Entry 14 of 16

File: USPT

Aug 29, 2000

US-PAT-NO: 6110331

DOCUMENT-IDENTIFIER: US 6110331 A

TITLE: Apparatus and system for fabricating lithographic stencil masks

DATE-ISSUED: August 29, 2000

INVENTOR-INFORMATION:

NAME

CITY

STATE

ZIP CODE

COUNTRY

Rolfson; J. Brett

Boise ID

US-CL-CURRENT: 204/224M; 134/182, 134/94.1, 134/99.1

#### ABSTRACT:

A method, apparatus and system for fabricating a stencil mask for ion beam and electron beam lithography are provided. The stencil mask includes a silicon substrate, a membrane formed from the substrate, and a mask pattern formed by through openings in the membrane. The method includes defining the mask pattern and membrane area using semiconductor fabrication processes, and then forming the membrane by back side etching the substrate. The apparatus is configured to electrochemically wet etch the substrate, and to equalize pressure on either side of the substrate during the etch process. The system includes an ion implanter for defining a membrane area on the substrate, optical or e-beam pattern generators for patterning various masks on the substrate, a reactive ion etcher for etching the mask pattern in the substrate, and the apparatus for etching the back side of the substrate.

11 Claims, 17 Drawing figures Exemplary Claim Number: 1 Number of Drawing Sheets: 3

Full Title Citation Front Review	Classification Date Reference Draw Ds

15. Document ID: US 5862823 A

L12: Entry 15 of 16

File: USPT

Jan 26, 1999

US-PAT-NO: 5862823

DOCUMENT-IDENTIFIER: US 5862823 A

TITLE: Substrate cleaning method and a substrate <u>cleaning apparatus</u>

DATE-ISSUED: January 26, 1999

INVENTOR-INFORMATION:

NAME CITY STATE ZIP CODE COUNTRY

Kamikawa; Yuji Kumamoto-ken JP Shindo; Naoki Nirasaki JP

US-CL-CURRENT: <u>134/182</u>; <u>134/1.3</u>, <u>134/186</u>, <u>134/34</u>, <u>134/61</u>, <u>134/902</u>, <u>15/302</u>, <u>15/77</u>

#### ABSTRACT:

The substrate cleaning method for performing cleaning processing on a plurality of substrates disposed such that front surfaces of the substrates on which a circuit pattern is to be formed extend substantially in a vertical direction. This method includes a step of picking up substrates contained in a cassette, all together, from the cassette, a step of making front surfaces of adjacent substrates face each other without bringing the front surfaces into contact with each other, while making back surfaces of adjacent substrates face each other without bringing the back surfaces into contact with each other, the front surfaces of the adjacent substrates being situated with a pitch interval L.sub.1 interposed therebetween, and the pitch interval being set to be larger than a pitch interval L.sub.2 interposed between the back surfaces of the adjacent substrates, a step of dipping the plurality of substrates thus disposed, all together, into a chemical solution, and a step of making the chemical solution flow between the front surfaces of adjacent substrates of the plurality of substrates, facing each other, and between the back surfaces of adjacent substrates of the plurality of substrates, facing each other.

11 Claims, 23 Drawing figures Exemplary Claim Number: 1 Number of Drawing Sheets: 15

Full   Title   Citation   Front   Review   Classification   Date   Reference	Claims   KWC   Draw De

16. Document ID: US 5069235 A

L12: Entry 16 of 16 File: USPT Dec 3, 1991

US-PAT-NO: 5069235

DOCUMENT-IDENTIFIER: US 5069235 A

TITLE: Apparatus for cleaning and rinsing wafers

DATE-ISSUED: December 3, 1991

INVENTOR-INFORMATION:

NAME CITY STATE ZIP CODE COUNTRY

Vetter; William L. American Fork UT Mortensen; Dennis L. Sandy UT

US-CL-CURRENT: <u>134/113</u>; <u>134/182</u>, <u>134/186</u>, <u>134/902</u>

#### ABSTRACT:

Apparatus for cleaning and rinsing wafers is disclosed. The apparatus includes an inner tank contained within an outer tank. The inner tank has an open top forming a weir edge around the entire top of the tank. A bottom opening in the inner tank is covered by a dump door. The inner tank is contoured so that its cross-sectional area decreases in a direction toward the bottom of the tank. Sprayer manifolds are positioned slightly above the top edge of the inner tank to spray water into the inner tank. Wafers are positioned in the inner tank on a support plate. Manifolds below the support plate allow filling of the tank with water and nitrogen gas. The dump door is opened or closed by a pneumatic piston depending on whether the inner tank is being dumped or filled. A controller operates the apparatus to cycle through a predetermined program including dump, partial dump, cascade and spraying cycles. A monitoring system withdraws water from the outer tank and monitors the water for particular characteristics including resistivity, conductivity and redox potential.

16 Claims, 12 Drawing figures Exemplary Claim Number: 1 Number of Drawing Sheets: 5

Title   Citation   Front   Review   Classification   Date   Reference	Claims ∴K0
Generate Collection Print Fwd Refs 8kwd Refs	Generate
Term	Documents
134/183	426
134/183S	0
134/182	690
134/182S	0
"134/99.1"	547
134/99.1S	0
(((134/183 OR "134/99.1" OR 134/182).CCLS.) AND 10).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	16
(L10 AND (134/183 OR 134/182 OR 134/99.1).CCLS. ).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	16

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## **WEST Search History**

Hide Items Restore Clear Cancel

DATE: Monday, September 13, 2004

Hide?	Set Name	Query	Hit Count
	DB=PGPP	B, USPT, USOC, EPAB, JPAB, DWPI, TDBD; PLUR=YES	S; OP=ADJ
	L12	110 and (134/183 or 134/182 or 134/99.1).ccls.	16
	L11	L9 and (single type)	13
	L10	L9 and single\$	1227
	L9	L8 and semiconductor	3202
	L8	cleaning apparatus	29396
	L7	L5 and concrete	18
. 🗖	L6	L5 and (concrete waste)	0
	L5	L4 and (not adher\$)	312
	L4	L3 and polymer\$	502
	L3	L2 and liner	3003
	L2	220/\$.ccls. and container	40904
	L1	220/\$.ccls. and (washout container)	0

**END OF SEARCH HISTORY**